VLSI Testing
Scan Design

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E0-286: Testing and Verification of SoC Design

Lecture – 16
Cyclic Circuit Example

Modulo-3 counter

s-graph

F1

F2
Modulo-3 Counter

- Cyclic structure – Sequential depth is undefined.
- Circuit is not initializable. No tests can be generated for any stuck-at fault.
- After expanding the circuit to $9^{N_{ff}} = 81$, or fewer, time-frames ATPG program calls any given target fault untestable.
- Circuit can only be functionally tested by multiple observations.
- Functional tests, when simulated, give no fault coverage.
Adding Initializing Hardware

Initializable modulo-3 counter

CNT

CLR

F1

F2

Z

s-a-0

s-a-1

s-a-1

s-a-1

s-a-1

s-a-1

s-a-1

s-a-1

Untestable fault

Potentially detectable fault

s - graph

F1

F2
Difficulties in Seq. ATPG

- Poor initializability.
- Poor controllability/observability of state variables.
- Gate count, number of flip-flops, and sequential depth do not explain the problem.
- Cycles are mainly responsible for complexity.

An ATPG experiment:

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Number of gates</th>
<th>Number of flip-flops</th>
<th>Sequential depth</th>
<th>ATPG CPU s</th>
<th>Fault coverage</th>
</tr>
</thead>
<tbody>
<tr>
<td>TLC</td>
<td>355</td>
<td>21</td>
<td>14*</td>
<td>1,247</td>
<td>89.01%</td>
</tr>
<tr>
<td>Chip A</td>
<td>1,112</td>
<td>39</td>
<td>14</td>
<td>269</td>
<td>98.80%</td>
</tr>
</tbody>
</table>

* Maximum number of flip-flops on a PI to PO path
## Benchmark Circuits

<table>
<thead>
<tr>
<th>Circuit</th>
<th>s1196</th>
<th>s1238</th>
<th>s1488</th>
<th>s1494</th>
</tr>
</thead>
<tbody>
<tr>
<td>PI</td>
<td>14</td>
<td>14</td>
<td>8</td>
<td>8</td>
</tr>
<tr>
<td>PO</td>
<td>14</td>
<td>14</td>
<td>19</td>
<td>19</td>
</tr>
<tr>
<td>FF</td>
<td>18</td>
<td>18</td>
<td>6</td>
<td>6</td>
</tr>
<tr>
<td>Gates</td>
<td>529</td>
<td>508</td>
<td>653</td>
<td>647</td>
</tr>
<tr>
<td>Structure</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sequential depth</td>
<td>4</td>
<td>4</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Total faults</td>
<td>1242</td>
<td>1355</td>
<td>1486</td>
<td>1506</td>
</tr>
<tr>
<td>Detected faults</td>
<td>1239</td>
<td>1283</td>
<td>1384</td>
<td>1379</td>
</tr>
<tr>
<td>Potentially detected faults</td>
<td>0</td>
<td>0</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>Untestable faults</td>
<td>3</td>
<td>72</td>
<td>26</td>
<td>30</td>
</tr>
<tr>
<td>Abandoned faults</td>
<td>0</td>
<td>0</td>
<td>76</td>
<td>97</td>
</tr>
<tr>
<td>Fault coverage (%)</td>
<td>99.8</td>
<td>94.7</td>
<td>93.1</td>
<td>91.6</td>
</tr>
<tr>
<td>Fault efficiency (%)</td>
<td>100.0</td>
<td>100.0</td>
<td>94.8</td>
<td>93.4</td>
</tr>
<tr>
<td>Max. sequence length</td>
<td>3</td>
<td>3</td>
<td>24</td>
<td>28</td>
</tr>
<tr>
<td>Total test vectors</td>
<td>313</td>
<td>308</td>
<td>525</td>
<td>559</td>
</tr>
<tr>
<td>Gentest CPU s (Sparc 2)</td>
<td>10</td>
<td>15</td>
<td>19941</td>
<td>19183</td>
</tr>
</tbody>
</table>
Scan Design

- Circuit is designed using pre-specified design rules.
- Test structure (hardware) is added to the verified design:
  - Add a *test control* (TC) primary input.
  - Replace flip-flops by *scan flip-flops* (SFF) and connect to form one or more shift registers in the test mode.
  - Make input/output of each scan shift register controllable/observable from PI/PO.
- Use combinational ATPG to obtain tests for all testable faults in the combinational logic.
- Add shift register tests and convert ATPG tests into scan sequences for use in manufacturing test.
Scan Flip-Flop (SFF)

- D flip-flop
- MUX

Master latch
Slave latch

- Normal mode, D selected
- Scan mode, SD selected

Logic overhead

CK

Master open Slave open

TC

Normal mode, D selected Scan mode, SD selected
Level-Sensitive Scan-Design Flip-Flop (LSSD-SFF)

Master latch

Slave latch

D flip-flop

MCK

SCK

SD

TCK

Logic overhead

MCK

TCK

MCK

TCK

SCK

Normal mode

Scan mode

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Adding Scan Structure

PI → Combinational logic → PO

Not shown: CK or MCK/SCK feed all SFFs.

TC or TCK → SCANIN → SFF → SCANOUT
Comb. Test Vectors

Combination logic

Present state

Next state

PI

SCANNIN

TC

I1

I2

S1

S2

O1

O2

N1

N2

PO

SCANOUT

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Comb. Test Vectors

Sequence length = \((n_{\text{comb}} + 1) n_{\text{sff}} + n_{\text{comb}}\) clock periods

\(n_{\text{comb}} = \text{number of combinational vectors}\)

\(n_{\text{sff}} = \text{number of scan flip-flops}\)

Don’t care or random bits
Testing Scan Register

- Scan register must be tested prior to application of scan test sequences.
- A shift sequence 00110011 . . . of length \( n_{sff} + 4 \) in scan mode (TC=0) produces 00, 01, 11 and 10 transitions in all flip-flops and observes the result at SCANOUT output.
- Total scan test length: \( (n_{comb} + 2) n_{sff} + n_{comb} + 4 \) clock periods.
- Example: 2,000 scan flip-flops, 500 comb. vectors, total scan test length \( \sim 10^6 \) clocks.
- Multiple scan registers reduce test length.
Multiple Scan Registers

- Scan flip-flops can be distributed among any number of shift registers, each having a separate *scanin* and *scanout* pin.
- Test sequence length is determined by the longest scan shift register.
- Just one *test control* (TC) pin is essential.

DIAGRAM:

- PI/SCANIN
- Combinational logic
- SFF
- TC
- CK
- MUX
- PO/SCANOUT
Scan Overheads

- IO pins: One pin necessary.
- Area overhead:
  \[
  \text{Gate overhead} = \left[ 4 \frac{n_{\text{sff}}}{n_g + 10n_{\text{ff}}} \right] \times 100\%,
  \]
  where \(n_g = \text{comb. gates}; n_{\text{ff}} = \text{flip-flops}\).
  Example – \(n_g = 100\text{k gates}, n_{\text{ff}} = 2\text{k flip-flops}\),
  overhead = 6.7%.
  More accurate estimate must consider scan wiring and layout area.
- Performance overhead:
  Multiplexer delay added in combinational path; approx. two gate-delays.
  Flip-flop output loading due to one additional fanout; approx. 5-6%.
Hierarchical Scan

- Scan flip-flops are chained within subnetworks before chaining subnetworks.

- Advantages:
  - Automatic scan insertion in netlist
  - Circuit hierarchy preserved - helps in debugging and design changes

- Disadvantage: Non-optimum chip layout.
Optimum Scan Layout

Active areas: XY and X’Y’
### ATPG Example: S5378

<table>
<thead>
<tr>
<th>Category</th>
<th>Original</th>
<th>Full-scan</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of combinational gates</td>
<td>2,781</td>
<td>2,781</td>
</tr>
<tr>
<td>Number of non-scan flip-flops (10 gates each)</td>
<td>179</td>
<td>0</td>
</tr>
<tr>
<td>Number of scan flip-flops (14 gates each)</td>
<td>0</td>
<td>179</td>
</tr>
<tr>
<td>Gate overhead</td>
<td>0.0%</td>
<td>15.66%</td>
</tr>
<tr>
<td>Number of faults</td>
<td>4,603</td>
<td>4,603</td>
</tr>
<tr>
<td>PI/PO for ATPG</td>
<td>35/49</td>
<td>214/228</td>
</tr>
<tr>
<td>Fault coverage</td>
<td>70.0%</td>
<td>99.1%</td>
</tr>
<tr>
<td>Fault efficiency</td>
<td>70.9%</td>
<td>100.0%</td>
</tr>
<tr>
<td>CPU time on SUN Ultra II, 200MHz processor</td>
<td>5,533 s</td>
<td>5 s</td>
</tr>
<tr>
<td>Number of ATPG vectors</td>
<td>414</td>
<td>585</td>
</tr>
<tr>
<td>Scan sequence length</td>
<td>414</td>
<td>105,662</td>
</tr>
</tbody>
</table>
Scan Design Rules

- Use only clocked D-type of flip-flops for all state variables.
- At least one PI pin must be available for test; more pins, if available, can be used.
- All clocks must be controlled from PIs.
- Clocks must not feed data inputs of flip-flops.
Correcting a Rule Violation

- All clocks must be controlled from PIs.

Comb. logic

D1

Q

FF

Comb. logic

D2

Comb. logic

D1

D2

Q

FF

Comb. logic

CK

CK
Thank You