VLSI Testing

Introduction

Virendra Singh
Indian Institute of Science
Bangalore
virendra@computer.org

E0 286: Test & Verification of SoC Design
Lecture - 1
VLSI Realization Process

Customer's need

Determine requirements

Write specifications

Design synthesis and Verification

Test development

Fabrication

Manufacturing test

Chips to customer
Definitions

- **Design synthesis:** Given an I/O function, develop a procedure to manufacture a device using known materials and processes.

- **Verification:** Predictive analysis to ensure that the synthesized design, when manufactured, will perform the given I/O function.

- **Test:** A manufacturing step that ensures that the physical device, manufactured from the synthesized design, has no manufacturing defect.
Verification vs. Test

Verification
- Verifies correctness of design.
- Performed by simulation, hardware emulation, or formal methods.
- Performed once prior to manufacturing.
- Responsible for quality of design.

Test
- Verifies correctness of manufactured hardware.
- Two-part process:
  1. Test generation: software process executed once during design
  2. Test application: electrical tests applied to hardware
- Test application performed on every manufactured device.
- Responsible for quality of devices.
Problems of Ideal Tests

- Ideal tests detect all defects produced in the manufacturing process.
- Ideal tests pass all functionally good devices.
- Very large numbers and varieties of possible defects need to be tested.
- Difficult to generate tests for some real defects. *Defect-oriented testing* is an open problem.
Real Tests

- Based on analyzable fault models, which may not map on real defects.
- Incomplete coverage of modeled faults due to high complexity.
- Some good chips are rejected. The fraction (or percentage) of such chips is called the *yield loss*.
- Some bad chips pass tests. The fraction (or percentage) of bad chips among all passing chips is called the *defect level*.
Testing as Filter Process

- **Good chips**
  - $\text{Prob}(\text{good}) = y$
  - $\text{Prob}(\text{pass test}) = \text{high}$
  - $\text{Prob}(\text{fail test}) = \text{low}$
  - Mostly good chips

- **Fabricated chips**

- **Defective chips**
  - $\text{Prob}(\text{bad}) = 1 - y$
  - $\text{Prob}(\text{fail test}) = \text{high}$
  - $\text{Prob}(\text{pass test}) = \text{low}$
  - Mostly bad chips

- **Tested chips**

**Roles of Testing**

- **Detection**: Determination whether or not the device under test (DUT) has some fault.
- **Diagnosis**: Identification of a specific fault that is present on DUT.
- **Device characterization**: Determination and correction of errors in design and/or test procedure.
- **Failure mode analysis** (FMA): Determination of manufacturing process errors that may have caused defects on the DUT.
Costs of Testing

- **Design for testability (DFT)**
  - Chip area overhead and yield reduction
  - Performance overhead
- **Software processes of test**
  - Test generation and fault simulation
  - Test programming and debugging
- **Manufacturing test**
  - *Automatic test equipment* (ATE) capital cost
  - Test center operational cost
DFT refers to hardware design styles or added hardware that reduces test generation complexity.

Motivation: Test generation complexity increases exponentially with the size of the circuit.

Example: Test hardware applies tests to blocks A and B and to internal bus; avoids test generation for combined A and B blocks.
Testing Principle

INPUT PATTERNS
---11
---00
-----
-----
---01

OUTPUT RESPONSES
10---
00---
-----
-----
01---

DIGITAL CIRCUIT

STORAGE CORRECT RESPONSE

COMPARATOR

TEST RESULT
ADVANTEST Model
T6682 ATE
Cost of Manufacturing Testing

- 0.5-1.0GHz; analog instruments; 1,024 digital pins: ATE purchase price
  = $1.2M + 1,024 x $3,000 = $4.272M
- Running cost (five-year linear depreciation)
  = Depreciation + Maintenance + Operation
  = $0.854M + $0.085M + $0.5M
  = $1.439M/year
- Test cost (24 hour ATE operation)
  = $1.439M/(365 x 24 x 3,600)
  = 4.5 cents/second
Cost Analysis Graph

- Fixed cost
- Variable cost
- Average cost

Miles Driven

- 0
- 50k
- 100k
- 150k
- 200k

Fixed, Total and Variable Costs ($)

- 0
- 20,000
- 25,000
- 40,000

Average Cost (cents)

- 0
- 50
- 100

Jan 16, 2008
A Modern VLSI Device
System-on-a-chip (SOC)

Data terminal

DSP core

RAM ROM

Interface logic

Mixed-signal Codec

Transmission medium